

**Remarks/ Arguments**

In response to the Office Action mailed April 7, 2004, Applicants respectfully request that the Examiner reconsider the objections to the specification and the claims.

Claims 1-20 remain.

Claims 3 and 15 are being amended.

Claim 15 stands objected-to on the basis of a grammatical error. Applicants have amended Claim 15 to correct this formality.

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ober* (U.S. Patent 6,665,802) (hereinafter "the *Ober* reference"). Applicants respectfully traverse these rejections.

The *Ober* reference does not teach or suggest circuits and systems having digital circuitry disposed on one power plane and analog circuitry disposed on another power plane. Specifically, the *Ober* reference does not teach or suggest either multiple-power planes or analog and digital circuitry fabricated on the same chip and on separate power planes.

The *Ober* reference merely teaches a system in which individual circuit blocks can be powered-down or have their clock signal forced into a static state. (The *Ober* reference, Col. 9, Lines 49 – 58). No mention is made of power planes, and specifically individually controllable power planes.

The Examiner correctly admits that the *Ober* reference does not teach an on-chip analog subsystem.


No new matter has been added; the claims have been merely amended to more particularly claim the subject matter Applicants believes is inventive. Applicants respectfully submit that the Claims as they now stand are patentably distinct over the art cited during the prosecution thereof.

With the addition of no new claims, no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 20-0821.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 969-1749.

Respectfully submitted,

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